This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (currently amended) The multi-package module of claim [[1]] 17 wherein the processor comprises a CPU.

6. (currently amended) The multi-package module of claim [[1]] 17 wherein the processor comprises a GPU.

7. (currently amended) The multi-package module of claim [[1]] 17 wherein the processor comprises an ASIC.

8. (currently amended) The multi-package module of claim [[1]] 17 wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate.

9. (currently amended) The multi-package module of claim [[1]] 17 wherein the first package is a BGA package.

10. (currently amended) The multi-package module of claim [[8]] 17 wherein the first package is a LGA package.

11. (canceled)

12. (canceled)

13. (canceled)

14. (canceled)

15. (canceled)

16. (canceled)

17. (currently amended) A multi-package module, comprising
a module substrate,
a processor mounted on a portion of a first surface of the module substrate, and
a plurality of memory package stacks disposed over portions of the module substrate adjacent the portion to which the processor is mounted, wherein each memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate, wherein the plurality of memory package stacks comprise a memory package assembly, wherein a common memory package assembly substrate comprises the package stack substrate for each of the plurality of memory package stacks, and ~~The multi-package module of claim 16~~ wherein the common memory assembly substrate spans the portion of the module substrate onto which the processor is mounted.

18. (currently amended) The multi-package module of claim [[16]] 17 wherein an opening is provided in the common memory assembly substrate over the processor.

19. (original) The multi-package module of claim 18 wherein a heat slug is mounted onto the processor, and the opening in the common memory assembly substrate accommodates the heat slug.

20. (original) The multi-package module of claim 19 wherein the heat slug occupies the volume between a top surface of the processor and an upper limit of the module.

21. (original) The multi-package module of claim 20 wherein a heat spreader is mounted onto a top surface of the heat slug.

22. (original) The multi-package module of claim 9 wherein an array of balls provides for electrical interconnection of each BGA memory package to a surface of the memory stack substrate.

23. (withdrawn) The multi-package module of claim 22 wherein an array of bumps provides for electrical interconnection of each BGA memory package to a surface of the memory stack substrate.

24. (withdrawn) The multi-package module of claim 9 wherein an upper BGA package in the stack is connected to an upper surface of the memory stack substrate and a lower BGA package in the stack is inverted and connected to a lower surface of the memory stack substrate.

25. (original) The multi-package module of claim 10 wherein z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

26. (currently amended) A multi-package module, comprising
a module substrate,
a processor mounted on a portion of a first surface of the module substrate, and
a memory package stack disposed over a portion of the module substrate adjacent the portion to which the processor is mounted, wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate, wherein the first package is a LGA package, and

wherein ~~The multi-package module of claim 10 wherein the~~ LGA memory packages in the stack are stacked in like orientation, and are separated by spacers to provide relief for z-interconnect wire bond loops between a lower package in the stack and the module substrate.

27. (original) The multi-package module of claim [[10]] 26 wherein each LGA memory package in the stack is electrically connected to the memory stack substrate by wire bonding, and the z-interconnect between the memory package and the module substrate is made by wire bonding between the memory stack substrate and the module substrate.

28. (currently amended) A multi-package module, comprising
a module substrate,
a processor mounted on a portion of a first surface of the module substrate, and
a memory package stack disposed over a portion of the module substrate adjacent the portion to which the processor is mounted, wherein the memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate, wherein the first package is a LGA package, and ~~The multi-package module of claim 10~~ wherein a lower LGA package in the stack is affixed to and is wire bond connected to a lower surface of the memory stack substrate and an upper LGA package in the stack is inverted and affixed to and is wire bond connected to an upper surface of the memory stack substrate.

29. (canceled)

30. (canceled)

31. (canceled)

32. (canceled)

33. (currently amended) The multi-package module of claim [[29]] 41 wherein the processor comprises a CPU.

34. (currently amended) The multi-package module of claim [[29]] 41 wherein the processor comprises a GPU.

35. (currently amended) The multi-package module of claim [[29]] 41 wherein the processor comprises an ASIC.

36. (canceled)

37. (currently amended) The multi-package module of claim [[36]] 41 wherein the first package is a BGA package.

38. (currently amended) The multi-package module of claim [[36]] 41 wherein the first package is a LGA package.

39. (canceled)

40. (canceled)

41. (currently amended) A multi-package module comprising
a module substrate,
a processor mounted on a portion of a first surface of the module substrate, and
a plurality of memory package stacks disposed in part over a portion of the module substrate adjacent the portion to which the processor is mounted, wherein each memory package stack comprises a first package affixed onto a first surface of a package stack substrate and a second package affixed onto a second surface of the package stack substrate, wherein the plurality of memory package stacks comprise a memory package assembly, and wherein a common memory package assembly substrate comprises the package stack substrate for each of the

plurality of memory package stacks and ~~The multi-package module of claim 40~~ wherein the common memory assembly substrate spans the portion of the module substrate onto which the processor is mounted.

42. (original) The multi-package module of claim 41 wherein an opening is provided in the common memory assembly substrate over the processor.

43. (original) The multi-package module of claim 42 wherein a heat slug is mounted onto the processor, and the opening in the common memory assembly substrate accommodates the heat slug.

44. (original) The multi-package module of claim 43 wherein the heat slug occupies the volume between a top surface of the processor and an upper limit of the module.

45. (original) The multi-package module of claim 44 wherein a heat spreader is mounted onto a top surface of the heat slug.

46. (currently amended) The multi-package module of claim [[40]] 41 wherein the memory packages comprise BGA memory packages and wherein an array of balls provides for electrical interconnection of each BGA memory package to a surface of the common memory assembly substrate.

47. (currently amended) The multi-package module of claim [[40]] 41 wherein the memory packages comprise BGA memory packages and an array of bumps provides for electrical interconnection of each BGA memory package to a surface of the common memory assembly substrate.

48. (currently amended) The multi-package module of claim [[40]] 41 wherein the memory packages comprise BGA packages and wherein an upper BGA package in the stack is connected

to an upper surface of the common memory assembly substrate and a lower BGA package in the stack is inverted and connected to a lower surface of the common memory assembly substrate.

49. (currently amended) The multi-package module of claim [[29]] 41 wherein the memory packages comprise LGA memory packages.

50. (original) The multi-package module of claim 49 wherein z-interconnection between the LGA memory packages and the module substrate is made by wire bonding between each LGA memory package substrate and the module substrate.

51. (original) The multi-package module of claim 49 wherein the LGA memory packages in the stack are stacked in like orientation, and are separated by spacers to provide relief for z-interconnect wire bond loops between a lower package in the stack and the module substrate.

52. (currently amended) The multi-package module of claim [[40]] 41 wherein each LGA memory package is electrically connected to the common memory assembly substrate by wire bonding, and the z-interconnect between the memory package assembly and the module substrate is made by wire bonding between the common memory assembly substrate and the module substrate.

53. (currently amended) The multi-package module of claim [[40]] 41 wherein a lower LGA package is affixed to and is wire bond connected to a lower surface of the common memory assembly substrate and an upper LGA package is inverted and affixed to and is wire bond connected to an upper surface of the common memory assembly substrate.

54. (currently amended) The multi-package module of claim [[31]] 41, comprising two said memory package stacks, one each disposed on opposite sides of the processor.

55. (currently amended) The multi-package module of claim [[31]] 41, comprising four said memory package stacks, two each disposed on opposite sides of the processor.

56. (canceled)

57. (canceled)

58. (canceled)